IN THE SPECIFICATION

On page 1-56, following the title, please insert: --This is a continuation of U.S. Patent Application No. 08/484,918, filed June 7, 1995, which is now U.S. Patent No. 5,809,336, issued September 15, 1998.--

IN THE CLAIMS

Please amend the Claims as follows:

1. (amended) A microprocessor integrated circuit comprising:

a program-controlled processing unit operative in accordance with a sequence of program instructions;

a memory coupled to said processing unit and capable of storing information provided by said processing unit;

a plurality of column latches coupled to the processing unit and the memory, wherein, during a read operation, a row of bits are read from the memory and stored in the column latch; and

a variable speed system clock having an output coupled to said processing unit;

said processing unit, said variable speed system clock, said plurality of column latches, and said memory fabricated on a single substrate, said memory using a greater area of said single substrate than said processing unit, said memory further using a majority of a total area of said single substrate.

2. (amended) The microprocessor integrated circuit of claim 1 wherein said memory is dynamic random-access memory.

3. (amended) The microprocessor integrated circuit of claim 1 wherein said memory is static random-access memory.

4. (amended) A microprocessor integrated circuit comprising:

a processing unit disposed upon an integrated circuit substrate, said processing unit operating in accordance with a predefined sequence of program instructions;